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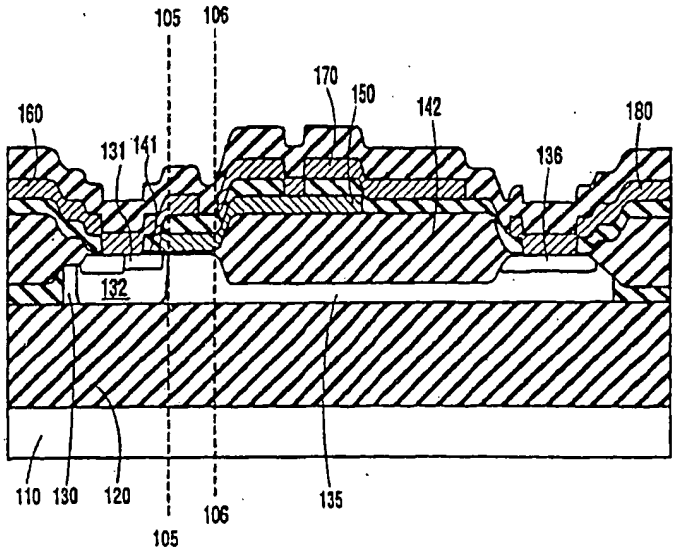
(54) Title: A HIGH VOLTAGE THIN FILM TRANSISTOR WITH IMPROVED ON-STATE CHARACTERISTICS AND METHOD FOR MAKING SAME



(57) Abstract

The present invention is directed to an SOI LDMOS device having improved current handling capability, particularly in the source-follower mode, while maintaining an improved breakdown voltage capability. The improvement in current handling capability is achieved in a first embodiment by introducing an offset region between the source and thin drift regions. The offset region achieves an offset between the onset of the linear doping profile and the thinning of the SOI layer that results in the thin drift region. In a second embodiment a further increase in the current handling capability of an SOI device is achieved by fabricating an oxide layer over the offset region, with the thickness of the oxide layer varying up to about half the thickness of the oxide layer fabricated over the thin drift region.

A high voltage thin film transistor with improved on-state characteristics and method for making same.

I. FIELD OF THE INVENTION

The present invention comprises a high voltage, thin film semiconductor-on-insulator (SOI) device with improved current handling capability when operating in the on-state. In particular, the present invention comprises specific SOI device architectures, and methods for making such devices, that introduce an offset region of varying thickness between the body and thin drift regions that significantly improves the current handling capability of SOI devices.

II. BACKGROUND OF THE INVENTION

The present invention relates to integrated circuit devices which are adapted for high voltage applications and, in particular, integrated circuit devices which are manufactured by the use of semiconductor-on-insulator (SOI) technology and which exhibit improved on-state current handling capabilities while maintaining improved off-state voltage breakdown properties.

Prior high voltage transistors have long been used to switch high voltages. When using these devices, it has been necessary to employ an associated control circuit (preferably an integrated circuit in complex applications) to control the switching function of the high voltage transistor. Associated control circuits typically operate at much lower voltages than high voltage transistors. For many practical reasons, including the difference in operating voltages, low voltage control circuits and high voltage transistors had at one time been fabricated in separate devices.

In order to achieve the related goals of maximum packaging efficiency and total part number reduction, it became desirable to fabricate high voltage transistors and associated control circuits in integrated circuits. Fabrication in single integrated circuits requires that the low voltage sections of these circuits be electrically isolated from the high voltage portions, and that the circuits manifest sufficient current handling capability for the given application.

These requirements concern two distinct operating modes of high voltage transistor integrated circuits -- the off-state and the on-state. The off-state performance is measured by breakdown voltage capability. The on-state performance is measured by on-

When the source electrode is biased positive (Vs) with respect to the substrate (which is at zero, or ground potential), part of the drift region of the device becomes depleted, thus reducing the cross-sectional area available for current flow, so that the on-resistance increases. Moreover, the silicon substrate acts as an electric-field plate which causes the current to saturate at high drain voltages. The depletion layer within the drift region lowers the magnitude of saturated current.

Increasing layer thicknesses uniformly will not increase the power handling capability of the device since it is only in thin film layers that a linear doping profile increases breakdown voltage capability. Such limitations have heretofore limited the usefulness of thin-film SOI devices where relatively high current handling capability was sought.

III. SUMMARY OF THE INVENTION

It is therefore an object of the present invention to increase the current-and-power-handling capability of a thin film, high voltage, SOI device while maintaining the desirable voltage breakdown properties of the device.

It is therefore another object of the present invention to decrease the on-resistance of a thin film, high voltage, SOI device while maintaining the desirable voltage breakdown properties of the device.

It is therefore a further object of the present invention to increase the current-and-power- handling capability of a thin film, high voltage, SOI device without unacceptably increasing device dimensions.

It is therefore yet another object of the present invention to decrease the on-resistance of thin film, high voltage, SOI devices without unacceptably increasing the device dimensions.

It is therefore a still further object of the present invention to increase the current-and-power-handling capability of a thin film, high voltage, SOI device when the device is operating in the source follower mode.

It is therefore an object of the present invention to decrease the on-resistance of a thin film, high voltage, SOI device when the device is operating in the source follower mode.

It is therefore another object of the present invention to provide a thin film, high voltage, SOI device that has improved current-and-power-handling capability and is economical to manufacture.

offset region and drift regions are oxide layers. The thickness of the oxide layer above the offset region varies up to about half the thickness of the oxide layer over the drift region. A linear doping profile is provided in the offset and drift regions to provide a high breakdown voltage capability for the device. Fabrication of an oxide layer over the offset region allows the lateral extent of the offset region to be further increased, thereby further improving the source follower current handling capability of the device, while still maintaining the desirable breakdown voltage properties of the device.

The methods of the present invention that accomplish an improvement in the source-follower current handling capability of the SOI device include fabrication techniques that comprise additional fabrication steps that introduce an offset region in the thin film SOI layer between the body region and the thin drift region. These fabrication steps have the effect of displacing the onset of the drift region thinning with respect to the onset of the linear doping profile. Additional methods of the present invention comprise fabrication steps that form an oxide layer over the offset region having a thickness of about half the oxide layer thickness deposited over the thin drift region. Fabrication of an oxide layer over the offset region allows the lateral extent of the offset region to be increased, thereby further increasing the source-follower current handling capability of the device without degrading the breakdown voltage capability of the device.

IV. BRIEF DESCRIPTION OF THE DRAWINGS

The above and other objects and advantages of this invention will be apparent upon consideration of the following detailed description, taken in conjunction with the accompanying drawings in which:

FIG. 1 is a cross-sectional view of a prior art thin film, high voltage, SOI transistor;

FIG. 2 depicts in plan view a typical half-bridge circuit comprising a pair of thin film, high voltage, SOI transistors, one of which is operating in a source-follower mode;

FIG. 3 depicts a cross-sectional view of a first embodiment of the present invention;

FIG. 4 depicts a cross-sectional view of a second embodiment of the present invention;

FIG. 5 depicts a graph of the drain current versus drain voltage for the two embodiments of the present invention depicted in FIGS. 3 and 4 in comparison to the prior art device depicted in FIG. 1;

the source follower transistor 94 can be biased up to 700 volts depending on operating conditions.

When the source electrode is biased positive (Vs) with respect to the substrate (which is at ground or zero potential), a portion 33 of the drift region 35 adjacent to the body region 32 of the device becomes depleted, thus reducing the cross-sectional area available for current flow, with the result that the on-resistance increases. Moreover, the silicon substrate acts as an electric field plate, which causes the current to saturate at high drain voltages. The depletion layer within the drift region lowers the magnitude of the saturated current. Curve (a) of FIG. 5 depicts the drain current vs. drain voltage characteristic for a device made in accordance with the prior art and shows the relatively poor current handling capability of the device. The present invention solves these problems and thereby improves the current handling capability of these devices in the following manner.

B. FIRST EMBODIMENT

FIG. 3 depicts a first embodiment of the present invention. The transistor comprises a substrate 110, an oxide layer 120, an epitaxial film layer 130, a source electrode 160, a gate electrode 170 and a drain electrode 180. Starting with the source region 131, the thin film layer 130 further comprises in lateral sequence from left to right a source region 131, a body region 132, an offset region 134, a drift region 135 and a drain region 136. Formed above thin film layer 130 are a gate oxide layer 141 and a drift region insulating layer 142. Fabricated above the gate oxide layer 141 and drift region insulating layer 142 layers is a polysilicon gate 150. In FIG. 1, the onset of the drift region thinning and the onset of the linear doping profile coincided at origin 5. In the device of FIG. 3, while the linear doping profile begins at origin 105, the onset of the drift region thinning does not coincide with the origin 105, but instead is offset by a distance D, representing the lateral distance between reference line 105 and reference line 106. By introducing an offset region 134 having a thickness greater than the thin drift region 135, the cross-sectional area available for current flow adjacent to the body region 132 is significantly increased over the device of FIG. 1.

The introduction of an offset region 134 results in a significant increase in the source-follower saturated current flow, as shown in curve (b) of FIG. 5 for a 2 micron offset, without compromising the high voltage breakdown properties of the SOI device structure. This results in a device which can deliver high power levels to a load in the source-follower mode. This device structure can be used over a wide voltage (hence application) range, e.g., up to 1100 V. In this voltage range, typical device dimensions are: SOI layer thickness: 0.25

available for current flow in region 33 of the device of FIG. 1, thereby substantially decreasing the saturation current flow of the device.

The relative effect of increasing layer thickness can be determined by treating the offset region 134 of FIG. 3 as a voltage-controlled resistor. The saturated current density then can be expressed as:

$$J_{sat} \sim q\, v_{sat}\, (t_{soi} - w)Q/q\, t_{soi} \qquad (1)$$

where Q is the background charge level, t_{soi} is the SOI layer thickness in the offset region 134 or region 33, v_{sat} is the saturated velocity and W is the depletion layer width from the substrate MOS capacitor due to the source-follower bias. The maximum depletion layer width at any point can be expressed as:

$$w(x) = [(4\ esi\ t_{soi}(x)\ Vf(x)/Q(x))]^{1/2} \qquad (2)$$

where Vf is the Fermi potential along the SOI/buried oxide interface. Since J_{sat} is proportional now to $t_{soi} - t_{soi}^{1/2}$, an increase in SOI layer thicknesses, represented by the relative thickness difference between the offset region 134 of the device of FIG. 3 and the thickness of region 33 of the device of FIG. 1 will increase J_{sat}. The t_{soi} in the offset region 134 of FIG. 3 should be greater than the maximum depletion width from the MOS capacitor, and the thicker t_{soi}, the larger the saturation current.

Thus it has been demonstrated that increasing the SOI layer thickness by offsetting the drift region oxide layer mask with respect to the origin of the linear doping profile improves the source-low and source-high ohmic and saturation current density. The maximum length of offset which can be used is determined by relative SOI and oxide layer thicknesses and the ratio of critical to average lateral electric field in the device structure.

As shown, the saturation current density is directly proportional to the background charge level in the offset region. Increasing the background doping level will result in significant increases in saturation current, as the ohmic conduction increases, and the net effect of the depletion region from the substrate MOS at source-high bias is smaller, resulting in a larger cross-section for current flow.

C. SECOND EMBODIMENT

FIG. 4 depicts a second embodiment of the present invention. The transistor comprises a substrate 210, an oxide layer 220, an epitaxial film layer 230, a source electrode 260, a gate electrode 270 and a drain electrode 280. Starting with the source region 231, the thin film layer 230 further comprises in lateral sequence from left to right a source region 231, a body region 232, an offset region 234, a drift region 235 and a drain region 236. Formed

First, thinning the SOI layer in the offset region reduces the contribution of a vertical breakdown path, thus the addition of the offset region does not degrade the breakdown voltage. Second, growth of an oxide which is a significant portion of the drift region oxide layer thickness shapes the electric field in this region of the device, thus rounding off the electric field peaks which can increase the breakdown voltage. This forms a structure that more nearly approximates an ideal gated diode structure. Third, growing a thick oxide in the offset region can be used to remove defects which remain from the formation of the drift region oxide layer, thus significantly improving gate oxide integrity.

D. FABRICATION METHODS

The structure of FIG. 4 for a device having an offset region 6 microns long, a drift region approximately 44 microns long, and a breakdown voltage of 700 volts may be manufactured employing techniques used to fabricate lateral MOS transistors, as follows. The following description is for a device optimized to achieve a breakdown voltage of 700 volts, and has a 3 micron thick buried oxide layer and 0.5 micron thick SOI layer. The starting SOI layer 230 is obtained by any of the standard techniques, such as, for example, zone melt recrystallization or direct bonding, is formed on the silicon substrate 210 with a buried oxide layer 220 interposed between the substrate 210 and the SOI layer 230. The silicon substrate 210 may be either n-type or p-type material. The SOI layer 230 has thickness less than 1.5 microns and resistivity greater than 0.1 ohm-cm. It may be fabricated from n-type or p-type material, but for the purposes of description it will be assumed that n-type material has been used.

The linear doping profile of the offset and drift region 234, 235 is introduced into the SOI layer 230 by ion implantation through a segmented mask 370 depicted in FIG. 6. The mask 370 is displaced vertically for clarity. The origin of the mask 370 coincides with reference origin 205, and may be formed by a photoresist layer patterned photolithographically by standard techniques. Thereafter phosphorous ions are implanted at an energy of 160 KeV. The photoresist mask 370 is provided with five openings of varying dimensions to enable the phosphorous ions to be implanted into the silicon layer 230 at varying amounts. The five openings in the photoresist mask with reference to origin 205 have their beginning and ending endpoints as follows: opening 371 begins at 8.25 microns and ends at 9.75 microns; opening 372 begins at 16.5 microns and ends at 19.5 microns; opening 373 begins at 25 microns and ends at 28.75 microns; opening 374 begins at 33.5 microns and ends at 38.5 microns; and opening 375 begins at 41.75 microns and ends at 71 microns. These five openings have

order of 2.2 microns. Similar steps are performed to form the offset region oxide layer 242, resulting in a suitably etched nitride layer 390 having a gap 395. As depicted in FIG. 8, a portion of this gap 395a extends beyond the drift region insulating layer 243 formed in the previous step, leaving the SOI layer 230 exposed in the region where the offset region oxide layer 242 is grown. The offset region oxide layer 242 is grown to a thickness of 1.0 micron. A buffered HF dip is used to remove any surface oxide which may have grown on the silicon nitride layer, and the nitride layer is removed with either reactive ion etching or wet chemical processing.

Prior to gate oxidation, a sacrificial oxidation is performed to remove any defects which may be present in the areas of the LOCOS step edge. These are referred to as "white ribbon" or "black belt" defects, and occur due to lateral nitridization of the silicon surface during the LOCOS oxidation. The severity of this defect is directly related to the total amount of oxide layer growth during the LOCOS process. The defects associated with the drift region oxide layer growth are more numerous and severe than those associated with the offset region oxide layer growth. To remove the defects, the pad oxide layer is stripped off with an HF solution, and a 0.1 micron or less wet (or dry) thermal oxide is grown on the surface of the SOI. This oxide is subsequently stripped off (hence sacrificial) and standard gate oxide processes can be employed.

The degree of nitridation is much worse for the drift region oxide layer growth 243 due to the fact that its oxidation thermal cycle is four times longer than for the offset region oxide layer 242. The second embodiment of this invention depicted in FIG. 4 which uses the offset region oxide layer growth 242 along with the drift region growth leads to much more robust gate oxide performance. The reason for this is the sacrificial oxidation is not always successful at removing the defects due to the drift region oxide layer growth, and the offset region oxide layer growth following the drift region oxide layer growth is very effective at removing the nitrided defect structure. Since the defect density is very small for the offset region oxide layer growth, the sacrificial oxide is very effective in removing the offset region oxide layer nitrided defects.

A 0.06 micron gate oxide layer 241 is grown over the surface of the wafer as depicted in FIG. 9. A photoresist mask 400 (again, all masking steps are vertically displaced for clarity, and previous steps are retained to illustrate the dimensional and spatial relationships among the steps) is provided to form the polysilicon layer. A layer of polysilicon 250 approximately 0.5 micron thick is deposited and the unmasked portion of this layer extending beyond the region represented by mask 400, is removed by reactive ion etching.

CLAIMS:

1. A high voltage, semiconductor-on-insulator electronic device, comprising:

a substrate (110);

a buried oxide layer (120) formed on the substrate, the buried oxide layer (120) having a buried oxide layer thickness;

a semiconductor layer (130) formed on the buried oxide layer (120), wherein the semiconductor layer (130) further comprises in lateral sequence a source region (131), a body region (132), an offset region (134), a thin drift region (135) and a drain region (136);

a drift region insulating layer (142) formed on the drift region (135) next to the gate oxide layer (141);

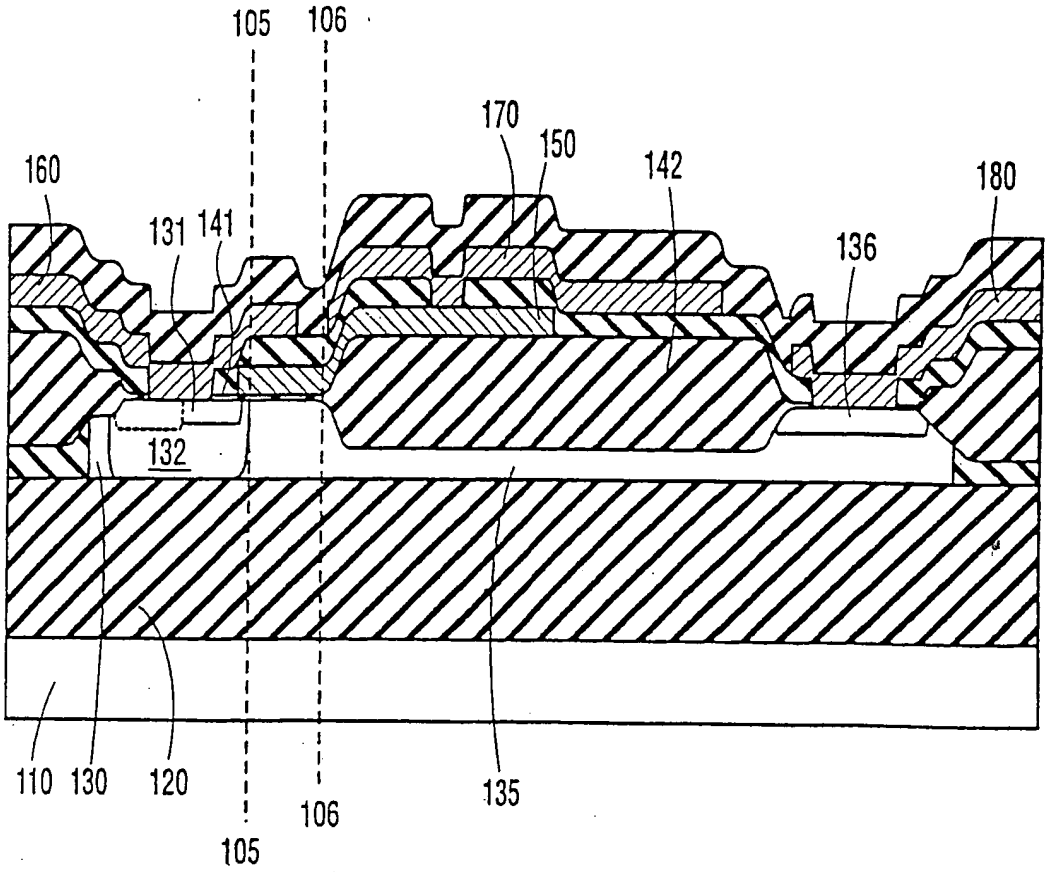
a further insulating layer formed on the source (131), body (132) and offset (134) regions next to the drift region insulating layer (142), which further insulating layer forms a gate oxide layer on at least the source (131) and body (132) regions;

a gate region (150) formed on the further insulating layer (242) and a portion of the drift region insulating layer (142);

the drift region (135) having a lateral length L and the offset region (134) having a lateral length D; the length L+D approximately describing the lateral distance between the body (132) and drain (136) regions; the drift region (135) having a thickness T_{drift}, and the offset region (134) having a thickness T_{offset}, both thicknesses T_{drift} and T_{offset} substantially perpendicular to said lateral dimension of said semiconductor layer (130); the thickness of the offset region T_{offset} being thicker than the thickness of the drift region T_{drift}; and the semiconductor layer (130) having a substantially linear doping profile between the body (132) and drain (136) regions, from a minimum value in the offset region (134) adjacent to the body region (132), to a maximum value in the thin drift region (135) adjacent to the drain region (136).

2. The high voltage, semiconductor-on-insulator electronic device of claim 1 wherein the drift region length L is substantially in the range of 10 to 100 microns; the offset region length D is substantially in the range of 2 to 6 microns; the buried oxide layer (120) has a thickness substantially in the range of 1 to 6 microns; the thickness of the drift region T_{drift} is

microns; the thickness of the offset region T_{offset} is substantially in the range of 1.0 to 1.5 microns; the thickness of the drift region insulating layer is substantially in the range of 2.0 to 3.0 microns; and the thickness of the offset region insulating layer is substantially in the range of 1.0 to 1.5 microns.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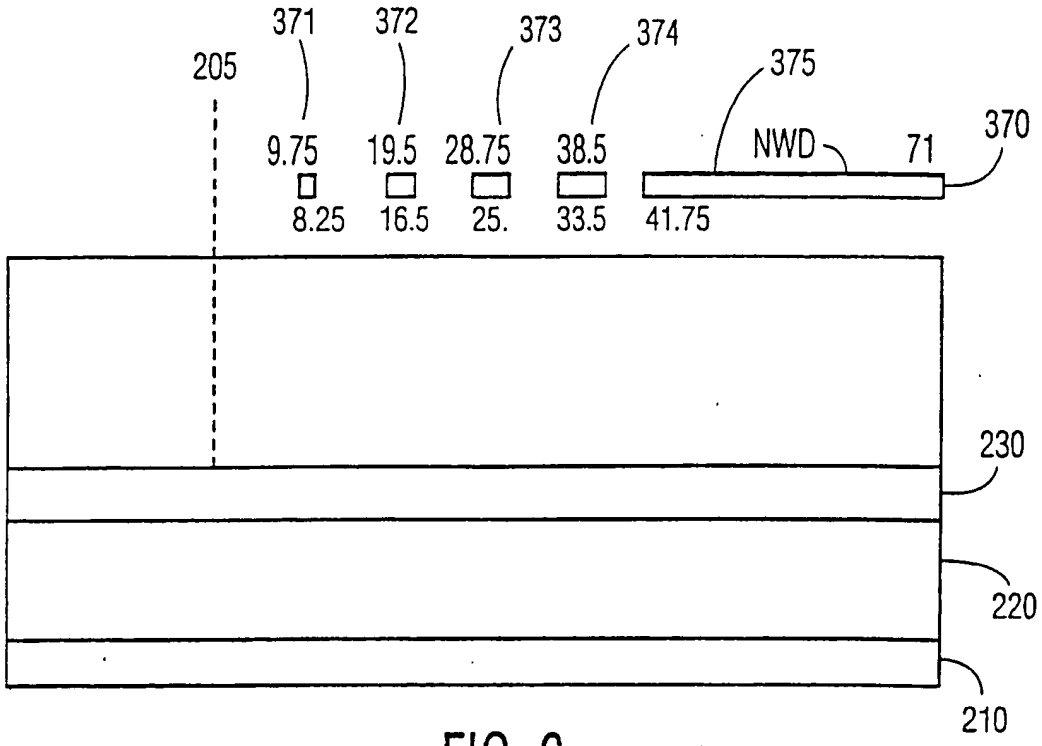
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FIG. 6

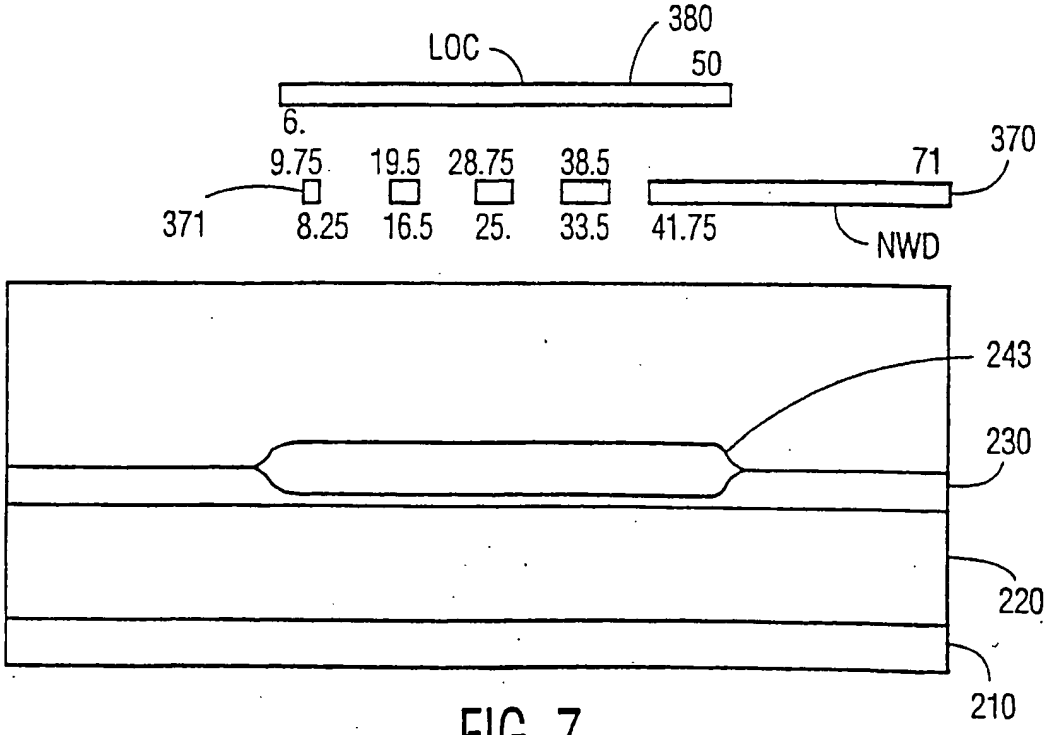
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FIG. 7

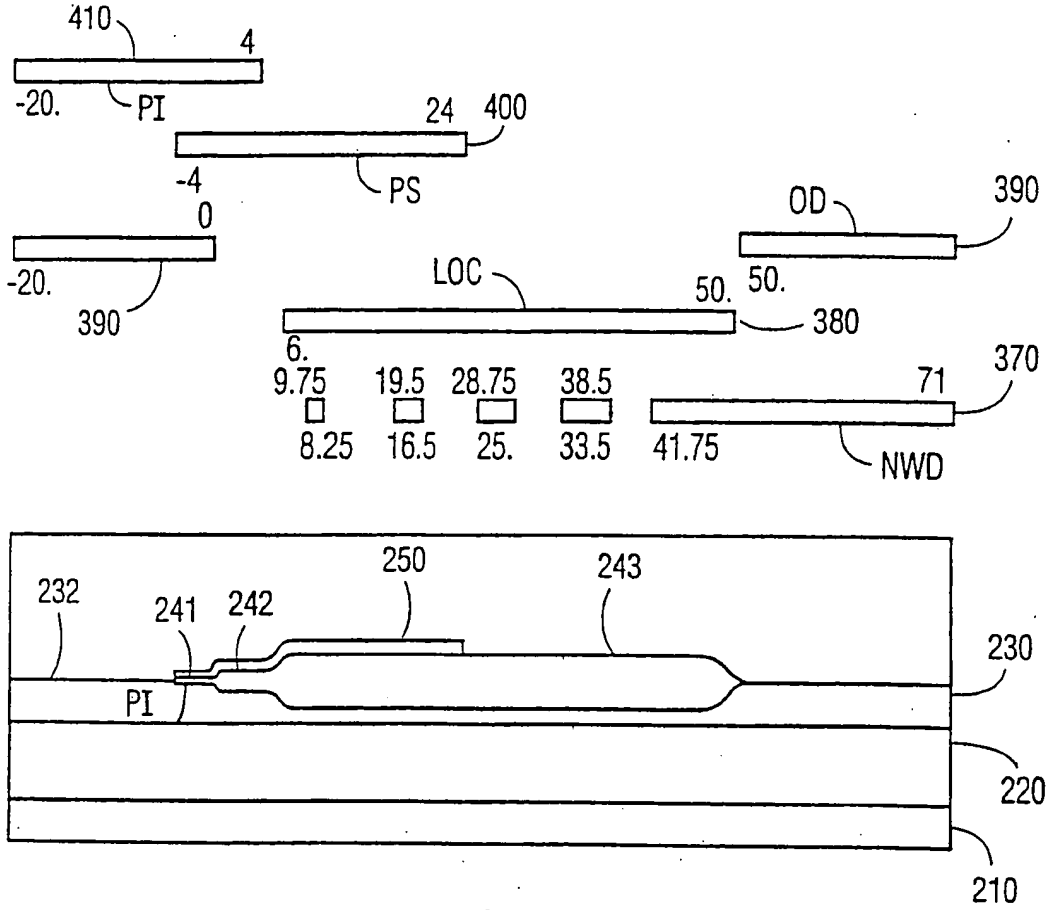
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FIG. 10